AMENDMENTS IN THE CLAIMS:

1. (Currently Amended) An LSI, comprising:

a RAM configured to store an intermediate code representing a command control string to be executed by a control section, and an encrypted intermediate code representing another command control string to be executed by the control section after first being decrypted;

a ROM configured to store cipher data used for decrypting the encrypted intermediate code, and to store an interpreter execution program that is configured to ~~interpret~~ generate the command control string from the intermediate code, and to decrypt and ~~interpret~~ generate the another command control string from the encrypted intermediate code, wherein the encrypted intermediate code includes address information indicating where the cipher data for decrypting the encrypted intermediate code is stored within the ROM, the address of the cipher data stored within the ROM being independent of where the encrypted intermediate code is stored in the RAM; and

a CPU configured to judge whether intermediate code obtained from the RAM is the intermediate code or the encrypted intermediate code, independent of where the intermediate code is stored in the RAM; configured to execute the interpreter execution program for ~~interpreting~~ generating the command control string from the intermediate code, and configured to execute the interpreter execution program for decrypting and ~~interpreting~~ generating the another command control string from the encrypted intermediate code by accessing the cipher data stored in the ROM at the address identified in the encrypted intermediate code.

2-3. (Canceled)

4. (Previously Presented) An LSI according to claim 1, further comprising:

a recording/reproduction head for recording/reproducing information on an optical disc; and

an optical disc control section for controlling a motor which drives the optical disc,

wherein the optical disc control section is comprised within the control section, and the RAM, the ROM, the CPU and the control section are formed on one chip.

5. (Currently Amended) An optical disc apparatus, comprising:

an execution section for executing an interpreter execution program that is configured to ~~interpret an intermediate code representing~~ generate a command control string from an intermediate code to be executed by a control section, and to decrypt and ~~interpret an encrypted intermediate code representing~~ generate another command control string from an encrypted intermediate code to be executed by the control section after first being decrypted, so as to generate a control command string, wherein the encrypted intermediate code includes address information indicating where cipher data for decrypting the encrypted intermediate code is stored within memory, the address of the cipher data stored within the memory being independent of where the encrypted intermediate code is stored within memory,

wherein the execution section judges whether intermediate code obtained from a memory is the intermediate code or the encrypted intermediate code independent of where the intermediate code is stored ~~in the~~ within memory; and

the control section for controlling recording/reproduction of information on an optical disc according to the control command string.

6. (Previously Presented) An optical disc apparatus according to claim 5, wherein the execution section includes:

a RAM for storing the encrypted intermediate code;

a ROM for storing the interpreter execution program; and

a CPU for controlling execution of the interpreter execution program.

7. (Original) An optical disc apparatus according to claim 6, wherein the RAM, the ROM, and the CPU are formed on one chip.

8. (Original) An optical disc apparatus according to claim 7, wherein the control section includes:

a recording/reproduction head for recording/reproducing information on the optical disc;

a motor for driving the optical disc; and

an optical disc control section for controlling the recording/reproduction head and the motor.

9. (Original) An optical disc apparatus according to claim 8, wherein the optical disc control section is formed on the one chip.

10. (Canceled)

11. (Previously Presented) An optical disc apparatus according to claim 6, wherein:

the RAM stores the encrypted intermediate code and the unencrypted intermediate code.

12. (Previously Presented) An LSI according to claim 1, wherein the RAM, the ROM, and the CPU are formed on one chip.

13. (Previously Presented) An LSI according to claim 1, wherein the intermediate code represents user customized command control strings, and the encrypted intermediate code represents vendor proprietary command control strings.

14. (Previously Presented) An optical disk apparatus according to claim 5, wherein the intermediate code represents user customized command control strings, and the encrypted intermediate code represents vendor proprietary command control strings.

15. (Previously Presented) An LSI according to claim 1, wherein the CPU judges whether intermediate code obtained from the RAM is the intermediate code or the encrypted intermediate code based on header information included in the intermediate code.

16. (Previously Presented) An LSI according to claim 15, wherein the header information is a flag.

17. (Currently Amended) An LSI, comprising:

a RAM configured to store an intermediate code representing a command control string to be executed by a control section, and an encrypted intermediate code representing another command control string to be executed by the control section after first being decrypted;

a ROM configured to store cipher data used for decrypting the encrypted intermediate code, and to store an interpreter execution program that is configured to ~~interpret~~ generate the command control string from the intermediate code, and to decrypt and ~~interpret~~ generate the another command control string from the encrypted intermediate code, wherein the encrypted intermediate code includes address information indicating where the cipher data for decrypting the encrypted intermediate code is stored within the ROM, the address of the cipher data stored within the ROM being independent of where the encrypted intermediate code is stored in the RAM; and

a CPU configured to judge whether intermediate code obtained from the RAM is the intermediate code or the encrypted intermediate code, independent of

where the intermediate code is stored in the RAM; and configured to control execution of the interpreter execution program based on a result of the judging.

18. (Previously Presented) An LSI according to claim 17, wherein the CPU judges whether intermediate code obtained from the RAM is the intermediate code or the encrypted intermediate code based on header information included in the intermediate code.

19. (Previously Presented) An LSI according to claim 18, wherein the header information is a flag.